REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended the claims in accordance with the Examiner's comments set forth in paragraphs 1-3 of the Office Action in order to address the pending objections thereto. Applicants wish to thank the Examiner for her assistance in overcoming the pending rejections. In addition, claims 1, 9 and 11 have been amended in an effort to further distinguish the present invention over the cited prior art. No new matter has been added.

Applicants wish to thank the Examiner for the indication of allowable subject matter being recited by claims 7 and 8.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of The Claims Under 35 U.S.C. § 103

Claims 1, 3, 5, 6, 9, 11 and 12 were rejected under 35 U.S.C. § 103 as being obvious over USP No. 5,471,409 to Tani. Applicants respectfully submit that the pending claims are patentable over Tani for at least the following reasons.

As explained in Applicants' previous response, in conventional verification systems, a large quantity of analytical data is required due to the fact that the verification is performed after ***all*** simulations are performed. This processing of large quantities of analytical data leads to various disadvantages as discussed on pages 7-9 of the specification. In contrast, in accordance with one aspect of the present invention, a simulation can be performed for a specific time and upon completion of said simulation, but not necessarily all simulations, the simulation result in

the specific time can be verified. Thereafter, the specific time can be incrementally increased and the next simulation can be performed at a subsequent time. Accordingly, in one aspect of the present invention, the specific time is repeatedly incrementally increased and the simulation process and verification of the simulation result are performed at each incremental increase in time. Claims 1, 9 and 11 have been amended in an effort to further clarify this aspect of the present invention and now recite that a "next" specific time utilized for a next simulating step and verification step is calculated by adding an infinitesimal time to the previous simulating step, and that the simulating step, the verifying step and the calculating step are repeatedly performed.

Thus, in accordance with an aspect of the present invention, after each of a plurality of simulating operation steps of the semiconductor circuit, which are performed with respect to time, the results of the simulating operation are stored, and the verification step is performed to determine whether or not the circuit elements satisfy voltage and/or current specifications. As a result of the foregoing process, the method of the present invention enables high-speed operation of the verification step, which determines whether or not the circuit elements being verified satisfy the loaded condition requirements. Moreover, the present invention can eliminate the requirement of having sufficient memory (e.g., a hard disk drive) for storing the results/data of the entire operation simulation.

Turning to the cited prior art, as also noted in the Applicants' previous response, Tani is completely silent as to performing a simulation for a specific time where the simulation result is verified, and thereafter incrementally increasing the specific time to perform a subsequent simulation and verification process. The verification process disclosed by Tani is basically a verification of ***static*** circuit delay information (such as fixed values of circuit operation delay times and fixed values of the signal propagating delay times due to resistances and capacitances

of the interconnects), and NOT a verification performed ***dynamically*** with respect to each specific time as performed by the present invention.

Further, the incremental delay ΔT disclosed in Tani is merely the difference between the delay time without factoring in the decrease in voltage and the delay time with the decrease in voltage being factored in (*see* col. 13, lines 19-27), but is NOT related to the verification and simulation while incrementally increasing the specification time. In other words, Tani determines precise signal propagation delay times that are utilized in the simulation process. This point is made clear by Tani which states that ΔT is determined:

> "so that the signal propagation delay time reflecting the voltage drop produced when each element operates can be set for each element of the logic circuit" col. 3, lines 41-45.

Importantly, however, even though Tani discloses determining precise signal propagation delay times, there is no disclosure that multiple simulation and verification processes are performed, much less at incremental steps in time.

Indeed, the portion of the specification cited in the Office Action as disclosing that Tani discloses performing simulation and verification operations at incremental time increments (col. 5, lines 3-17) also only discloses that the simulation process of Tani considers transient responses. This is done so as to allow for detection of circuit elements having simultaneous transient states and confirmation of whether or not such a condition would result in an unacceptable current requirement. However, once again, nowhere does Tani appear to disclose that a plurality of simulation and verification processes are performed at incremental steps in time. Tani just collects the foregoing data and performs a single simulation and verification process once the data is collected. There is nothing in the cited portion of Tani that would

suggest otherwise. The foregoing is also confirmed by the figures of Tani, none of which illustrate the simulation process being performed multiple times.

The disclosure at col. 12, lines 43-67 of Tani also confirms that Tani does not disclose the present invention as recited by claims 1, 9 or 11. As set forth therein, the process of Tani allows for determination of the elements that have a simultaneous state and utilizes this data in the simulation and verification process. However, once again, it appears that Tani only discloses a single verification process once the relevant data is obtained. Tani does not disclose or suggest the claimed invention in which the simulation process and verification of the simulation result are performed at incremental steps in time.

The Examiner is directed to M.P.E.P. § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, it is respectfully submitted that the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in the independent claims because Tani fails to disclose or suggest each of the limitations recited by the rejected claims.

III. The Rejection Of Claim 10 Under 35 U.S.C. § 103

Claim 10 was rejected under 35 U.S.C. § 103 as being obvious over USP No. 5,471,409 to Tani in view of JP 2000-132578 to Muraoka. Applicants respectfully submit that claim 10 is patentable over Tani and Muraoka for at least the following reasons.

Claim 10 is similar to claim 1 discussed above in that claim 10 recites an operation simulation means which computes voltage values or current values with respect to time, and a verification means that verifies the operation based on the data collected by the simulation means. Importantly, the verification means performs the verification process ***concurrently*** with the simulation performed by the operation simulation means. Thus, as with claim 1, claim 10 recites a simulation and verification process in which the simulation process and verification of the simulation result are each performed concurrently at various points in time.

Turning to the cited prior art, as discussed above, Tani merely discloses performing one simulation/verification process after all relevant data is collected. Tani does not appear to disclose performing multiple simulations and verifications concurrently at different times with respect to circuit operation. As such, Tani fails to render claim 10 obvious for essentially the same reasons as discussed above with respect to claim 1. Muraoka does not disclose or suggest the foregoing element of claim 10, and is not relied upon as doing so in the pending rejection. Thus, as each and every limitation must be disclosed or suggested by the cited prior art in order to establish a *prima facie* case of obviousness (M.P.E.P. § 2143.03), and Tani and Muraoka taken alone or in combination with one another fail to do so, it is respectfully submitted that claim 10 is patentable over the cited prior art.

IV. All Dependent Claims Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as the independent claims are patentable

for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

V. Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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